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Development of High Temperature Platinum TSVs

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Abstract

We report on harsh-environment-compatible Pt-TSVs forming ohmic contacts with a highly doped bulk silicon. They were developed as a part of a Single Wall Carbone NanoTube (SWCNT) resonator device with 3D-packaging. The fundamental properties of the TSVs, experimentally obtained with bulk Si instead of the real working device, are presented. Our concept for the device fabrication is "via first", followed by the nanodevice fabrication. As such, first ohmic contacts on silicon has been studied to be compatible with several harsh post-processing steps, including high temperature treatments—up to 850°C in air—and concentrated HF-based release steps. Then TSVs withstanding the aforesaid conditions have been developed. These interconnects are also of interest for MEMS devices operating at high temperature.

Keywords: Though Silicon Vias; high temperature; ohmic contacts; platinum, SOI, 3D-packaging

1. Introduction

Through Silicon Vias (TSVs) are nowadays giving a turning point in the MEMS packaging field. They provide electrical signal transportation through the bulk, allowing devices stacking and heterogeneous devices integration in a minimum of space and time. In a "Via first" approach, the TSVs are fabricated prior to the main electronic device in order that the characteristics of the main device are not influenced by the TSVs fabrication. But this approach requires that the TSVs have to be compatible with the processing steps necessary to make this main device.

In our case, the electronic device is a SWCNT resonator (fig.1) grown by CVD on Ferritin-based Fe catalyst [1], the growth process is carried out at 850°C. In a "Via first" approach, high temperature TSVs are required for its 3D-Packaging. Although studies on TSVs being compatible with high temperature treatment are not so many, they already shown that high temperature processing influences their properties [2, 3]; moreover, the commonly used Copper-TSVs [4] have their use limited in temperature. In order to achieve a SWCNT resonator with all electrical interconnects through TSVs, the following three points are the TSVs requirements:

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- Firstly, the TSVs should have ohmic contacts with the silicon device layer of a SOI wafer used for the resonator and peripheries;
- Secondly, since the CNT is very fragile and post-processing very limited, a “Via fist” approach was selected, with the TSVs still exhibiting an ohmic behaviour after the CNT growth process. The growth process considered is carried out at a temperature of 850°C, with eventually the presence of oxygen;
- Thirdly, the CNT resonator needs to be released by etching a SiO_2 sacrificial layer in HF (49%), which should be withstood by the TSVs.

This study is a proof of concept for the CNT resonator integrated with TSVs on SOI wafer, but the experiments have been done with bulk silicon.

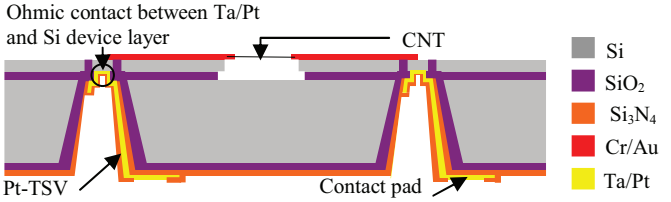

Fig. 1: Concept of the CNT resonator integrated with TSVs on SOI wafer (300 µm /1 µm /10 µm).

2. Metal-silicon ohmic contacts withstanding high temperature

Ohmic contact between the metal line formed in the via and the back of the silicon device to be created on the top is essential. We first investigated on this point. Ta/Pt metal combination was chosen as the conductive material owing to the good conductivity and stability at high temperature of the metals. Small test structures (Fig. 2(a)) were fabricated and annealed at different high temperatures. Different silicon substrates (0.015 Ω.cm/5 Ω.cm, N/P-type) were tested. The best results were obtained with the highly boron-doped silicon. Ohmic contacts were achieved right after the metal evaporation (Ta: 15 nm/ Pt: 235 nm) by e-beam and could withstand the annealing at 850°C for one hour in air (Fig. 2(b)).

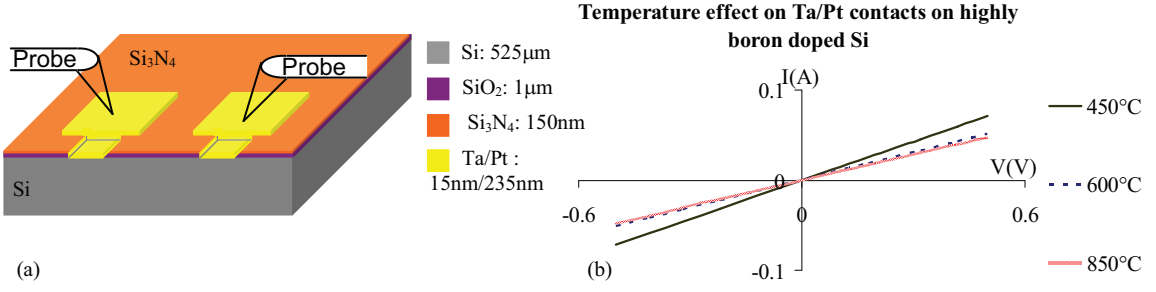

Fig. 2: a) Schematic of the test structure used for the study in temperature of Ta/Pt electrical contacts on silicon. The contact area is 50 µm x 50 µm, the pad size 175 µm x 175 µm, and the metal lifted-off on P-Si (0.015 Ω.cm). b) Corresponding I-V curves after annealing at different temperatures during 1h in air.

Although the contacts are still ohmic, the annealing slightly affected the characteristic of the contacts; the specific contact resistivity increased with the annealing temperature. After annealing for 1h at 450°C, the resistance increased from 50 $\mu\Omega\cdot cm^2$ to 130$\mu\Omega\cdot cm^2$ to 190$\mu\Omega\cdot cm^2$ when annealed respectively at 600°C and at 850°C with the same conditions.

3. Ohmic contacts passivation

Since the ohmic behaviour of the Ta/Pt-Si contact has to be preserved after the CNT growth and its release process in HF (49%), we considered a silicon nitride film deposited by LPCVD at 850°C as

passivation layer. Indeed, Si_3N_4 is an oxygen diffusion barrier; therefore it protects the contact area against oxidation at high temperature. Moreover, figure 3 shows that during the wet HF release process, the electrical properties of the contact are severely affected; therefore a passivation layer is mandatory. Figure 3 also shows that the Si_3N_4 film successfully protects the ohmic contacts during an annealing at high temperature during 1h in an oxygen atmosphere and also during a wet HF(49%) release step. As a result, 100nm of LPCVD-Si_3N_4 has been selected as passivation layer for Si-Ta/Pt contacts during the few minutes HF release step.

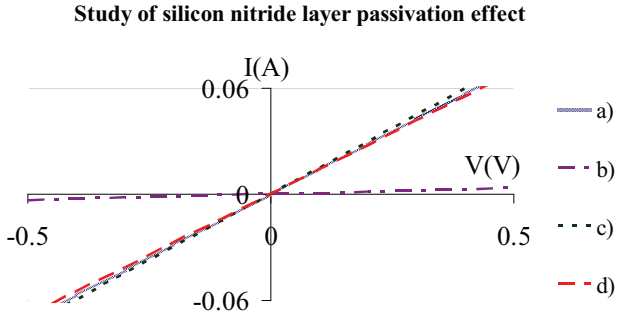

Fig. 3: I-V curves of Ta/Pt (15nm/235nm) contacts on a P-Si (0.015 Ω.cm). a) Ta/Pt contacts annealed at 850°C during 1h in air without any passivation layer b) Annealed at 850°C during 1h in air, and then subjected to wet HF during 3 min without passivation. c) Passivated with a silicon nitride layer (no annealing). d) Passivated with a silicon nitride layer, then annealed at 850°C during 1h in air.

The ohmic contact characteristics with a passivation layer have been studied. The ohmic contact is formed during the deposition of the silicon nitride passivation layer and the metallization is then stabilized; the contact resistivity remains around 80 $\mu\Omega.cm^2$ and does not vary during a subsequent annealing as long as the annealing is limited in time and the temperature is lower or equal to 850°C.

4. TSVs fabrication

After having identified passivated Ta/Pt metallization on highly boron-doped silicon wafer as our best parameters for contacts withstanding high temperature and wet HF processes, Pt-KOH-TSVs were fabricated as a proof of concept on oxidized silicon wafers; figure 4 shows the process details.

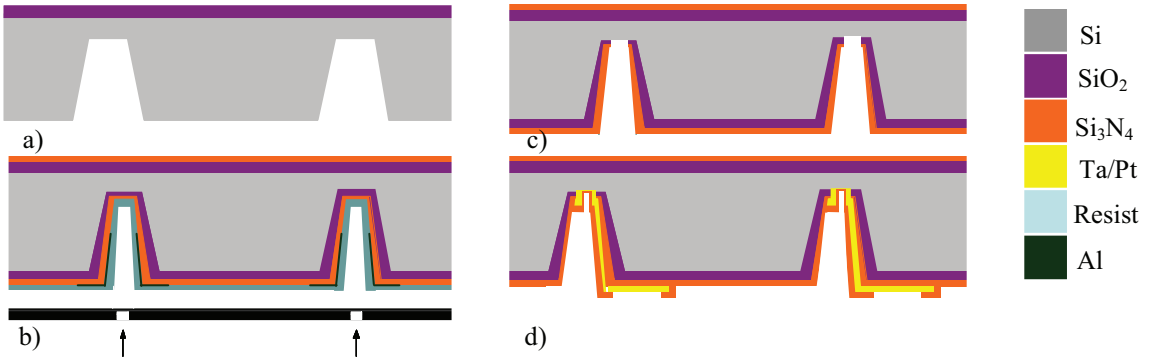

Fig. 4: Process flow for the KOH-Pt TSVs fabrication for demonstration.

300 µm- deep pits were etched by KOH in the silicon wafer (P-Si: 390µm, R=0.015 Ω.cm) The edges of the pits have been tapered by etching five more micrometers of Si in KOH but this time without any mask (Fig. 4a). Then the pits have been isolated with a 250 nm- thick SiO_2 layer; a 150 nm- thick LPCVD-Si_3N_4 layer has been added as diffusion barrier.

A backside lithography process has been realized to open contact windows on the silicon device layer. We choose the spray coating technique in order to have a better homogeneity of the resist inside the 300µm- deep cavities. But the main difficulty of this spray coating step is to cover the cavities edges with

the resist; we avoided that problem by adding before the spray coating a 300 nm- thick aluminium layer, evaporated only at the cavities edges, through a stencil mask. The Al layer is used as a mask to protect the edges of the cavities during the subsequent etching step (Fig.4b). After the backside lithography, the dielectric layers were etched to reach the highly-doped silicon at the bottom of the pits using a DRIE process (Fig. 4c). The top and backside of the wafer were electrically connected by evaporating the Ta/Pt (15nm/235nm) in the pits through a shadow mask by e-beam evaporation . 150 nm of silicon nitride can been deposited and patterned by LPCVD as passivation layer(Fig. 4d).

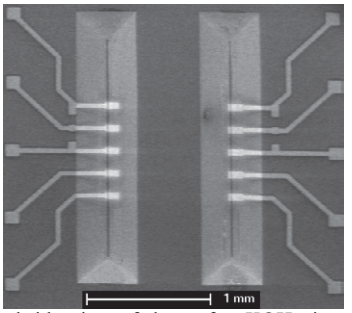

Fig. 5: Backside view of the wafer: KOH pits electrically insulated and electrical contacts on the silicon opened at the bottom.

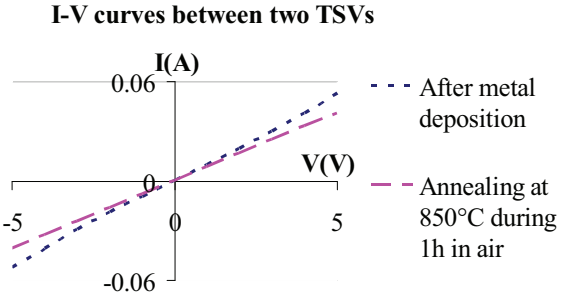

Fig. 6: I-V curves between two KOH-Pt TSVs without silicon nitride passivation.

Figure 6 shows that the TSVs exhibit an ohmic behaviour after the metal deposition; we verified that the ohmic behaviour of the TSVs is kept after annealing at high temperature (fig 6). Finally, the LPCVD-silicon nitride passivation layer can be deposited and patterned if required.

Conclusion

We have demonstrated a process for the fabrication of passivated high temperature Pt-TSVs with ohmic contacts on a silicon device layer of a SOI wafer. These interconnects are of interest for the 3D-packaging with a “via first” approach of delicate devices requiring processes in harsh conditions, such as the growth of SWCNTs, and also for MEMS devices operating at high temperature.

TSVs are nowadays crucial for RF-MEMS packaging, therefore the RF-parameters of these high temperature Pt-TSVs are going to be measured and optimized in future studies.

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